RICHI DUBEY

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EDUCATION

Birla Institute of Technology & Science, Pilani — Goa, India

B.E., Computer Science | Core CS GPA: 9.3 | Overall GPA: 8.84 — *2017 - June 2021*

- *K*ey Courses: Operating Systems (A-Grade), Computer Networks (A-Grade), Data Structures and Algorithms, Machine Learning, Artificial Intelligence, Real-Time Systems, Data Storage Technologies and Networking
- *A*wards: Merit Cum Need Scholarship (80% of Tuition Fees)

WORK EXPERIENCE

Fellow - CERN — *October 2022 – Present*

Health Safety and Environment (HSE) Department

- Leading the design and technical implementation of distributed and redundant SCADA systems by spearheading the development of REMUS, a comprehensive supervision system managing 1k+ diverse devices deployed in accelerator, experimental, and surface areas at CERN.
- Developing multi-threaded device drivers in C++ for REMUS and state-aware fault-tolerant networking programs for devices, resulting in optimized performance and robust networking capabilities across CERN's expansive network of sensors.
- Successfully enabling real-time acquisition and archival of 10,000,000 values per hour, while empowering remote device configuration for users and implementing advanced alarm triggers in the CERN Control Center (CCC) to promptly notify operators of critical events and ensure swift response.

Member Technical Staff - Oracle — *July 2021 – September 2022*

Oracle Cloud Infrastructure | Oracle Process Cloud Team

- Built highly secure, scalable, and high performance multi-tenant applications for the Oracle Cloud Infrastructure (OCI) by using microservice architecture that service more than 2 billion requests per month.
- Also played a crucial role in DevOps efforts, ensuring seamless deployment of applications across 50+ OCI data centers worldwide.
- Utilized a diverse tech stack, including Java, Spring, Spring Boot, SQL, Terraform, Docker, Kubernetes, Oracle Cloud, and Git to deliver cutting-edge solutions.

Research Intern - High-Performance Real-Time Lab, UNIMORE, Italy — *Jan 2021 – April 2021*

Undergraduate Thesis

- Explored innovative tools in Virtualization and Automation, gaining expertise in emerging technologies.
- Implemented a system for remote benchmarking of workloads in embedded systems by integrating the Workload Automation (WA) tool by ARM with the Jailhouse partitioning hypervisor on a custom Linux kernel.
- Significantly enhanced workload execution predictability and introduced real-time guarantees to mitigate contention in the shared memory hierarchy.

Research Software Developer - RTEMS Real-Time Operating System — *May 2020 – August 2020*

Google Summer of Code | More details here

- Contributed to RTEMS, a renowned real-time operating system extensively utilized in various domains, including NASA/ESA satellites, sports bikes, and particle accelerators across esteemed institutions like CERN, US DoE National Labs and various European facilities.
- Implemented the Strong Arbitrary Processor Affinity (APA) scheduler, a state-of-the-art scheduling algorithm that has not been implemented in a real-world operating system before.
- The Strong APA scheduler introduced the ability to dynamically relocate higher-priority tasks among processors, optimizing resource allocation by accommodating lower-priority tasks constrained by affinity requirements. The scheduler is proven to be able to schedule roughly **15-20%** more task sets than other schedulers when evaluated on benchmarks.

PUBLICATIONS

Work in Progress: Strong APA Scheduling in a Real-Time Operating System
Richi Dubey, Vijay Banerjee, Sena Hounsinou and Gedare Bloom
SIGBED International Conference on Embedded Software (EMSOFT) 2021.
Paper Link, Talk Link, Poster Link

Next-Generation Embedded Development Tools and Technologies – Virtualisation and Automation
Bachelor Thesis, at HiPeRT Lab | Paper Link

AWARDS

HERCULES Prize- edition 2019/2020 — University of Modena and Reggio Emilia, Italy *October 2020*
Awarded €4500 to work with Prof. Marko Bertogna on High-Performance Real-time Architecture for Low-Power Embedded Systems at HIPeRT Lab, Unimore, Italy.

McGill Summer Undergraduate Research in Engineering (SURE) Award — McGill University, Canada *May 2020*
Awarded $5,625.00 in Summer 2020 to work with Prof. Liboiron-Ladouceur on Photonic Hardware for AI.

OPEN SOURCE CONTRIBUTIONS

RTEMS: Code Contributions, Documentation Contributions | **Siemens S7200 C++ Driver**: Code Contributions

TECHNICAL BLOG

RTEMS with Richi — Visit here *May 2020 - Present*
I share my expertise in software development for real-time operating systems here.

RESEARCH PROJECTS

Approaches towards Censorship Circumvention BITS Pilani
September 2020 – November 2020

- Conducted a comprehensive review of the latest security software, Noctilucent, to explore and test various use cases of Encrypted Server Name Indication (ESNI) in TLS 1.3 as a means to circumvent censorship. Notably, TLS 1.3 is employed by nearly **30%** of all websites on the Internet and **59%** of websites hosted on Cloudflare.
- Established and configured a server on Microsoft Azure to evaluate security vulnerabilities in DNS over HTTPS (DoH) and other critical network security protocols.

Review of Mixed Criticality Systems BITS Pilani
August 2019 – December 2019

- Reviewed various scheduling algorithm like Global Preemptive EDF, Criticality Based EDF (CBEDF) etc. and various resource sharing protocols like Priority Ceiling Protocol (PCP), Priority Inheritance Protocol (PIP) etc.
- Implemented the Earliest Deadline First with Virtual Deadline (EDF-VD) Scheduling Algorithm by Prof. Baruah et al. in C

SKILLS

Programming Languages: C, C++, Java, Python 3, SQL **Systems**: Linux Kernel, RTEMS Real Time Kernel

POSITIONS OF RESPONSIBILITY

Teaching Assistant - Department of CS & IS BITS Pilani
Designed and conducted tutorials, graded papers and provided guidance to students for the core courses:

- Data Structure and Algorithm (Semester II, 2019 - 2020)
- Computer Programming (Semester II, 2019 - 2020)
- Logic in Computer Science (Semester I, 2019 - 2020)